UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,601	09/23/2003	Dureseti Chidambarrao	FIS920030186US1	9755

7590 07/12/2004

McGuireWoods LLP
Suite 1800
1750 Tyson Boulevard
McLean, VA 22102

EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/667,601	CHIDAMBARRAO ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/23/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-16 in the reply filed on April 15, 2004 is acknowledged.

Claim Objections

Claim11 is objected to because of the following informalities: In line 3, the examiner suggest changing "HF" to –Hf—since "Hf" is the recognized form of the element. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "deposited oxide" in lines 1 and 2-3. There is insufficient antecedent basis for this limitation in the claim. A deposited oxide has not been positively recited in claim 9 or the claim from which it depends.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-5, 12, and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle et al. (U.S. Patent No. 6,288,694).

Doyle et al. teaches in one embodiment the method of forming an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor on a semiconductor wafer, the method comprising:

covering the p-type transistor with a mask and creating voids such that tensile mechanical stresses are formed within a channel of the n-type transistor without creating additional tensile stresses in a channel of the p-type transistor (see Figures 5-7, column 4, lines 40-55, Figure 11, column 5, lines 5-25, and claims 1 and 5).

Doyle et al. does not teach in that embodiment that the voids are formed by oxidizing a portion of a gate polysilicon of the n-type transistor. Doyle discloses in an additional embodiment that voids are formed by oxidizing a portion of the gate polysilicon of the n-type transistor (see column 5, line 40 through column 6, line 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the voids by oxidizing a portion of the gate polysilicon since Doyle et al. teaches it is an alternative method of forming the voids that creates a tensile stress which increases the carrier mobility of the NMOS device.

In re claim 3 and 5, Doyle discloses the method wherein the step of oxidation is performed by using low temperature oxidation, about 25 degrees C to about 600 degrees C, as defined by applicant (see column 5, lines 60-65). The examiner notes

that the annealing step may be considered a part of the oxidation step since it allows for formation of the voids. Further, if the annealing process is not considered part of the oxidation step, then examiner notes that the oxidation step is performed at a temperature below that of the annealing temperature (400 degrees C), and thus is also considered a low temperature oxidation process.

In re claim 4, Doyle et al. discloses the method wherein the step of oxidation is performed by at least one of high pressure oxidation or atomic oxidation or plasma oxidation. The examiner notes that since oxygen atoms are being implanted it is considered an atomic oxidation step.

In re claim 12, Doyle et al. discloses the method of removing the mask used to cover the p-type field effect transistor (see column 5, lines 66-67).

In re claims 14 and 15, Doyle et al. does not disclose the range of tensile stress created in the n-type FET. The examiner notes that Applicant does not teach that the tensile stress range solve any stated problem or are for any particular purpose. Therefore, the tensile stress range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the NFET with a tensile stress range as claimed, since the invention would perform equally well as long as sufficient tensile stress is applied to the NMOS region to increase the carrier mobility, as Doyle et al. teaches, and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Claims 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle et al. (U.S. Patent No. 6,288,694) in view of Khan et al. (U.S. Patent No. 4,517,731).

Doyle et al. discloses the method as claimed and rejected above including forming a mask of photoresist, but does not disclose the method wherein the mask is made of nitride.

Khan et al. discloses the method wheirn a mask is made of nitride. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the mask of Doyle et al. with nitride since as Khan et al. teaches silicon nitride is less expensive, more reliable and much easier to work with as compared with the use of photoresist.

Claims 1, 3-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. (U.S. Patent No. 6,204,103) in view of Doyle et al. (U.S. Patent No. 6,288,694).

In re claims 1 and 16, Bai et al. discloses the method for forming an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor on a semiconductor wafer. Bai et al. does not disclose the method of covering the p-type transistor with a mask and oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor without creating additional tensile stresses in a channel of the p-

type transistor (see Figures 5-7, column 4, lines 40-55, Figure 11, column 5, lines 5-25, and claims 1 and 5).

Doyle et al. does not disclose the method of covering the p-type transistor with a mask and oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor without creating additional tensile stresses in a channel of the p-type transistor (see Figures 5-7, column 4, lines 40-55, Figure 11, column 5, line 5, through column 6, line 3, and claims 1 and 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to cover the p-type transistor with a mask and oxidize the gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor without creating additional tensile stresses in a channel of the p-type transistor because as Doyle teaches increasing the tensile stresses in the NMOS region while preventing the increasing of the tensile stresses in the PMOS region increases carrier mobility (see column 3, lines 20-25, an d column 5, line 40 through column 6, line 5).

In re claim 3 and 5, Doyle discloses the method wherein the step of oxidation is performed by using low temperature oxidation, about 25 degrees C to about 600 degrees C, as defined by applicant (see column 5, lines 60-65). The examiner notes that the annealing step may be considered a part of the oxidation step since it allows for formation of the voids. Further, if the annealing process is not considered part of the oxidation step, then examiner notes that the oxidation step is performed at a

temperature below that of the annealing temperature (400 degrees C), and thus is also considered a low temperature oxidation process.

In re claim 4, Doyle et al. discloses the method wherein the step of oxidation is performed by at least one of high pressure oxidation or atomic oxidation or plasma oxidation. The examiner notes that since oxygen atoms are being implanted it is considered an atomic oxidation step.

In re claim 6, Bai et al. discloses the method of forming a planarized oxide layer on the semiconductor wafer (1516).

In re claim 7 and 8, Bai et al. discloses the method comprising removing silicide (1505) material from above the gate polysilicon of the n-type field effect transistor, and wherein the step of removing silicide material form above the gate polysilicon of the n-type field effect transistor comprises etching the silicide material form above the gate polysilicon of the n-type field effect transistor (see column 6, lines 50-62).

In re claim 9, Bai et al. discloses the method further comprising removing deposited oxide (1516) from above the gate polysilicon of the -type field effect transistor by etching the deposited oxide from above the gate polysilicon of the n-type field effect transistor (see column 6, lines 50-55).

In re claim 10, Bai et al. discloses the method further comprising depositing silicide material on at least the portion of the gate polysilicon of the n-type field effect transistor (see column 6, line 63 through column 7, line 5).

In re claim 11, Bai et al. discloses the method wherein the step of depositing silicide forming material on at least the portion of the gate polysilicon of the n-type field

effect transistor comprises depositing at least one of Co, Hf, Mo, Ni, Pd_2, Pt, Ta, Ti, W, and Zr (see column 6, line 63 through column 7, line 5).

In re claim 12, Doyle et al. discloses the method of removing the mask used to cover the p-type field effect transistor (see column 5, lines 66-67).

In re claim 13, Bai et al. discloses the method of depositing at least one of a silicide material or a nitride cap on at least the gate polysilicon of the n-type field effect transistor and removing silicide material or the nitride cap form above the gate polysilicon of the no-type field effect transistor prior to performing the step of oxidizing (see column 6, lines 50-63).

In re claims 14 and 15, Doyle et al. does not disclose the range of tensile stress created in the n-type FET. The examiner notes that Applicant does not teach that the tensile stress range solve any stated problem or are for any particular purpose. Therefore, the tensile stress range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the NFET with a tensile stress range as claimed, since the invention would perform equally well as long as sufficient tensile stress is applied to the NMOS region to increase the carrier mobility, as Doyle et al. teaches, and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812